REMARKS/ARGUMENTS

In the Office Action mailed on June 8, 2009, claims 1, 2, 4, 5, 7, and 9-13 are rejected. In response, claims 1, 2, and 9 have been amended. Additionally, new claims 14-21 have been added. Applicant hereby requests reconsideration of the application in view of the claim amendments, the new claims, and the below-provided remarks.

Claim Rejections under 35 U.S.C. 103

Claims 1, 2, 4, 5, 7, 9, and 10 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hashimoto et al. (U.S. Pat. No. 5,587,962, hereinafter "Hashimoto") in view of Badger (U.S. Pat. No. 5,973,664). Claims 11-13 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hashimoto in view of Badger and further in view of Jaspers (U.S. Pat. No. 6,819,326 B2). However, Applicant respectfully submits that the pending claims are patentable over the cited references for the reasons provided below.

Independent Claim 1

Claim 1 has been amended to include the phrase "*storing a full table of line pointers for different sequences of video data to be displayed in the memory*" and to replace the phrase "a block of line pointers from a full table of line pointers in said memory is downloaded into said address table register means" with the phrase "*a block of line pointers from the full table of line pointers that is stored in said memory is downloaded into said address table register means*." Support for the amendments to claim 1 is found in Applicant's specification at, for example, original claim 4, Figs. 1 and 2, and page 5, lines 6 and 7.

As amended, claim 1 recites:

> "Method of operating a driving circuit for a display system, wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer, each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line, the method comprising:
> storing a full table of line pointers for different sequences of video data to be displayed in the memory; and

operating the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder, and in a second mode wherein a block of line pointers from the full table of line pointers that is stored in said memory is downloaded into said address table register means." (emphasis added)

Applicant respectfully asserts that Hashimoto in view of Badger fails to teach "*storing a full table of line pointers for different sequences of video data to be displayed in the memory*" and that "*a block of line pointers from the full table of line pointers that is stored in said memory is downloaded into said address table register means*" (emphasis added), as recited in amended claim 1.

Hashimoto teaches that an arbitration and control circuit (30) passes an address generated by an address generator (28a) to a memory array (24) so that data may be written into the memory array (24). (See Fig. 2 and column 5, lines 50-52 of Hashimoto). However, Hashimoto is silent on storing a full table of addresses of the data in the memory array (24) and then downloading a block of the full table of addresses stored in the memory array (24) into the address generators (28a), (28b). Additionally, Hashimoto teaches that an address generated by an address generator (28b) is transferred to the memory array (24) through the arbitration and control circuit (30) to cause data from the memory array (24) to be read into a read register (20b). (See Fig. 2 and the paragraph between column 5, line 66 and column 6, line 8 of Hashimoto). That is, Hashimoto teaches transferring addresses generated by address generators (28a), (28b) to the memory array (24) so as to write data into the memory array (24) and to read data from the memory array (24), respectively. However, Hashimoto fails to teach that any of the addresses transferred into the memory array (24) is downloaded into the address generators (28a), (28b). Thus, Applicant respectfully asserts that Hashimoto fails to teach the above-identified limitations of amended claim 1.

Badger teaches transferring an image (204) from a source memory (202) to a display memory (212) using an X_Counter and an Y_Counter. (See Fig. 8 and column 8, lines 16-39 of Badger). However, Badger fails to teach storing a full table of addresses of the data in the source memory (202) and then downloading a block of the full table of addresses stored in the memory array (24) into the X_Counter and the Y_Counter. Thus,

Applicant respectfully asserts that Badger fails to teach the above-identified limitations of amended claim 1.

Thus, Hashimoto in view of Badger fails to teach all the limitations of amended claim 1. As a result, Applicant respectfully asserts that amended claim 1 is patentable over Hashimoto in view of Badger.

Dependent Claim 11

Claim 11 depends from and incorporates all of the limitations of independent claim 1. Thus, Applicant respectfully asserts that claim 11 is allowable at least based on an allowable claim 1.

Independent Claim 2

Claim 2 has been amended in a similar fashion as claim 1. Support for the amendments to claim 2 can be found in Applicant's specification at, for example, original claim 4, Figs. 1 and 2, and page 5, lines 6 and 7. Because of the similarities between amended claim 1 and amended claim 2, Applicant respectfully asserts that the remarks provided above with regard to amended claim 1 apply also to amended claim 2. Accordingly, Applicant respectfully asserts that amended claim 2 is patentable over Hashimoto in view of Badger.

Dependent Claims 4, 5, 7, 10, and 12

Claims 4, 5, 7, 10, and 12 depend from and incorporate all of the limitations of independent claim 2. Thus, Applicant respectfully asserts that claims 4, 5, 7, 10, and 12 are allowable at least based on an allowable claim 2.

Independent Claim 9

Claim 9 has been amended in a similar fashion as claim 1. Support for the amendments to claim 9 can be found in Applicant's specification at, for example, original claim 4, Figs. 1 and 2, and page 5, lines 6 and 7. Because of the similarities between amended claim 1 and amended claim 9, Applicant respectfully asserts that the remarks provided above with regard to amended claim 1 apply also to amended claim 9.

Accordingly, Applicant respectfully asserts that amended claim 9 is patentable over Hashimoto in view of Badger.

Dependent Claim 13

Claim 13 depends from and incorporates all of the limitations of independent claim 9. Thus, Applicant respectfully asserts that claim 13 is allowable at least based on an allowable claim 9.

New Claims 14-21

New claims 14-21 have been added. Support for new claims 14-21 is found in Applicant's specification at, for example, page 6, lines 27-31. Claims 14, 15, 18, and 19 depend from and incorporate all of the limitations of independent claim 2. Claims 16, 17, 20, and 21 depend from and incorporate all of the limitations of independent claim 9. Thus, Applicant respectfully asserts that claims 14-21 are allowable at least based on allowable claims 2 and 9, respectively. Additionally, claims 14-21 may be allowable for further reasons, as described below.

Claims 14 and 16 recite that "*a line pointer relates to a part of a picture line, and wherein the pixel counter counts pixels of the part of the picture line*" (emphasis added). Claims 15 and 17 recite that "*a line pointer relates to a half of a picture line, and wherein the pixel counter counts pixels of the half of the picture line*" (emphasis added). Claims 18 and 20 recite that "*a line pointer relates to more than one picture line, and wherein the pixel counter counts pixels of the more than one picture line*" (emphasis added). Claims 19 and 21 recite that "*a line pointer relates to two picture lines, and wherein the pixel counter counts pixels of the two picture lines*" (emphasis added). Applicant respectfully asserts that Hashimoto, Badger, and Jaspers fail to teach the individual limitations of claims 14-21.

As described above, Hashimoto teaches that the address generators (28a), (28b) generate memory addresses to write data into the memory array (24) or to read data from the memory array (24). However, Applicant respectfully asserts that Hashimoto fails to teach that a row address generated by the address generators (28a), (28b) is related to a part of a picture line, in particular, a half of a picture line. Additionally, Applicant

respectfully asserts that Hashimoto also fails to teach that a row address generated by the address generators (28a), (28b) is related to more than one picture line, in particular, two picture lines. Thus, Applicant respectfully asserts that Hashimoto fails to teach the individual limitations of claims 14-21.

As described above, Badger teaches transferring the image (204) from the source memory (202) to the display memory (212) using an X_Counter and an Y_Counter. Badger also teaches that the Y_Counter holds the number of source image lines (302) that are left to be transferred. (See Fig. 8 and column 8, lines 22-28 of Badger). However, Applicant respectfully asserts that Badger fails to teach that the line count produced by the Y_Counter is related to a part of a source image line, in particular, a half of a source image line. Additionally, Applicant respectfully asserts that Badger also fails to teach that the line count produced by Y_Counter is related to more than one source image line, in particular, two source image lines. Thus, Applicant respectfully asserts that Badger fails to teach the individual limitations of claims 14-21.

Jaspers is cited for teaching the limitation "*each block of line pointers is limited to thirty two line pointers*" in claim 11 and the limitations "*the number of line pointers in the address table register means is limited to thirty two*" in claims 12 and 13. (See pages 8 and 9 of the Office Action). Jaspers teaches that a logical size of a memory device is such that it can keep the pixels from 32 video lines with 128 pixels each. (See column 7, lines 15-22 of Jaspers). However, Applicant respectfully asserts that Jaspers is silent on the individual limitations of claims 14-21.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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